Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HORMAZDYAR M. DALAL,
ALEXIS BITAILLOU, KENNETH M. FALLON,
GENE J. GAUDENZI, KENNETH R. HERMAN,
FREDERIC PIERRE, and GEORGES ROBERT

Appeal No. 1999-0725
Application 08/476,475[1]

ON BRIEF

Before CALVERT, BARRETT, and KRATZ, Administrative Patent Judges.

BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

[1] Application for patent filed June 7, 1995, entitled "Method For Forming Reflowed Solder Ball With Low Melting Point Metal Cap."

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-26.

We reverse.

BACKGROUND

The invention relates to a method of capping a solder ball with a layer of low melting point metal, as may be understood from claim 1, the sole independent claim, reproduced below.

> 1. A method of capping a solder ball with at least one layer of low melting point metal, said method comprises the steps of
>
> (a) forming said solder ball on a substrate,
>
> (b) placing a mask over said solder ball such that said mask surrounds a portion of said solder ball and such that a portion of said solder ball is exposed,
>
> (c) depositing at least one layer of a low melting point metal over said solder ball through said mask, such that at least a portion of said solder ball has a capping layer of said low melting point metal, and wherein the melting point of said low melting point metal is lower than the melting point of said solder ball.

THE PRIOR ART

The Examiner relies on the following prior art:

Noll	3,512,051	May 12, 1970
Melton et al. (Melton)	5,154,341	October 13, 1992

Eiji Horikoshi et al. JP 62-117346[2] May 28, 1987
(Japanese Patent Publication)

[2] A translation of this reference has been prepared by the U.S. Patent and Trademark Office and a copy of the translation accompanies this decision.

Rao R. Tummala and Eugene J. Rymaszewski, Section 6.3 Controlled Collapse Chip Connection (C4), Microelectronics Packaging Handbook (Van Nostrand Reinhold 1989) (hereinafter Microelectronics).[3]

THE REJECTION

Claims 1-20 and 22-26 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Japanese Patent Publication No. JP 62-117346 ('346 reference) or Noll in view of Appellants' admitted state of the prior art as shown in figure 6-14(c) of Microelectronics.

Claim 21 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over the '346 reference or Noll in view of Appellants'

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[3] The Examiner states that no date is given for this reference (Examiner's Answer, p. 3). Appellants cite the date as 1989 (specification, p. 3, line 26). We have determined the publication date to be December 2, 1988, the copyright registration date to be December 27, 1988, and the imprint date to be 1989 (in agreement with Appellants' citation), from the Copyright Office online database (at "http://www.copyright.gov"). The information is reproduced below, where DCRE is the date of creation, DPUB is the date of publication, DREG is the date of registration, and IMPR is the imprint date.

TITL: Microelectronics packaging handbook / edited by Rao R. Tummala, Eugene J. Rymaszewski; managing editor, Alan G. Klopfenstein.
IMPR: New York : VanNostrand Reinhold, c1989.
PHYS: 1194 p.
CLNA: VanNostrand Reinhold, a division of International Thomson Publishing Corporation
DCRE: 1988 DPUB: 2Dec88 DREG: 27Dec88
MISC: C.O. corres.
ECIF: 1/B/L

admitted state of the prior art as shown in figure 6-14(c) of Microelectronics, further in view of Melton.

We refer to the final rejection (Paper No. 9) and the examiner's answer (Paper No. 14) for a statement of the Examiner's position, and to the appeal brief (Paper No. 13) for Appellants' arguments thereagainst.

OPINION

Grouping of claims

Appellants state that the rejected claims do not stand or fall together (Br6). Appellants' reasons why the claims are separately patentable are that neither "'346 nor Noll either alone or in combination with another reference either anticipate or make obvious the inventions of [one of claims 2-26, wherein the claim recites . . .]" (Br6-12). This does not constitute an argument why the claims are separately patentable. See 37 CFR § 1.192(c)(7) (1997) ("Merely pointing out differences in what the claims cover is not an argument as to why the claims are separately patentable."). Appellants only argue the limitations of claims 1 and 21 separately. Thus, claims 1-20 and 22-26 will stand or fall together with claim 1 and claim 21 will stand or fall by itself.

Obviousness

It is necessary to begin with a definition of "solder ball," as defined in the specification (p. 11, lines 2-8):

> It should be noted that the term "solder ball" as used in conjunction with this invention means that the lead and tin have been combined and gone through at least one reflow cycle and formed a "solder ball". Therefore, it should be clear to a person skilled in the art that the invention is an improvement of these already formed solder balls or C4s.

The reflow cycle brings the solder to a spherical shape as shown in Appellants' figure 1 due to the surface tension of the solder.

In claim 1, the step of "(a) forming said solder ball on a substrate" is not found in the '346 reference and is not accounted for in the Examiner's rejection. The '346 reference[4] shows a high melting point metal 24 deposited on a pad 22 on the ceramic substrate 21 via a metal mask 23 at a thickness of 100 :m (translation, p. 7). Then a low melting point metal 25 is deposited on material 24 at a thickness of 20 :m via the mask 23 (translation, p. 7). This results in a solder "bump" consisting of a high melting point metal layer 24 and a low melting point metal layer 25. Respective solder bumps on a semiconductor chip 26 and a ceramic substrate 21 are mounted to face each other and the low melting point

[4] Figure 3 in the '346 reference appears to be the same as figure 6-20b of Microelectronics.

materials are selectively melted to join the bumps together (translation, p. 8). It is not disclosed that the high melting point metal layer 24 is reflowed to become a solder ball. The Examiner states that "[s]older balls (24) . . . are vapor deposited onto the solder heads [pads] (22)" (EA4), which assumes that metal layer elements 24 are solder balls. However, as shown in Microelectronics, discussed infra, solder can be deposited without forming a solder ball because heat is needed to reflow the solder into a ball. Accordingly, we find that the '346 reference does not disclose the claimed step of "(a) forming said solder ball on a substrate." Consequently, the '346 reference also does not disclose steps (b) and (c), which incorporate the reference to a solder ball. Furthermore, step (b) requires "placing a mask over said solder ball," which process step requires placing a mask over the existing solder ball of step (a) and the '346 reference does not show a separate step of placing a mask over an existing solder ball or element; the process of the '346 reference using a single mask to deposit both layers 24 and 25 does not meet the terms of step (b).

Noll discloses a spherically-shaped mass of high melting point solder 40 formed by dipping the crystal substrate having metal film 34 into molten solder. This metal volume 40 is considered a

solder ball because "when removed from the molten solder, the volume of solder which adheres to the film tends to take a shape which has minimum surface area" (col. 2, lines 69-71); i.e., it is formed into a ball shape from a liquid state, albeit not by reflowing a solid to a liquid state. Noll discloses that a thin film 50 of low melting point solder is formed by dipping the crystal 10 into a pot of solder (col. 3, lines 1-13). The capped solder ball in Noll is essentially identical to the capped solder ball in Appellants' figure 2; however, claim 1 is directed to the method of making. Noll does not disclose placing a mask over the solder ball as recited in claimed step (b) and does not disclose depositing a layer of low melting point metal over the solder ball through the mask as recited in claimed step (c).

Microelectronics discloses formation of a conventional solder ball or controlled collapse chip connection (C4). The lead and tin components are deposited in layers as shown in figure 6-14(c) (according to the legend; however, it is actually shown to the left of the label "(b)"). "Reflow in an H_2 ambient furnace at about 350°C melts and homogenizes the pad and brings it to a spherical shape." Page 378. The reflowed solder ball is shown in figure 6-14(d) (according to the legend; however, it is actually shown next to the label "(c)"). Thus, as deposited, the solder does not form a solder

ball. Microelectronics shows a mask having a knife edge approximately halfway between the upper and lower surfaces. Microelectronics does not disclose placing a mask over the solder ball as recited in claimed step (b) and does not disclose depositing a layer of low melting point metal over the solder ball through the mask as recited in claimed step (c).

Because the references do not teach depositing a layer of low melting point metal over a solder ball with a mask, we conclude that the Examiner has failed to establish a prima facie case of obviousness with respect to claim 1. The rejection of claims 1-20 and 22-26 is reversed.

Melton is applied to the rejection of claim 21. However, Melton does not cure the deficiencies of the rejection of claim 1. Accordingly, the rejection of claim 21 is reversed.

CONCLUSION

The rejections of claims 1-26 are reversed.

REVERSED

IAN A. CALVERT)
Administrative Patent Judge)

LEE E. BARRETT Administrative Patent Judge	BOARD OF PATENT APPEALS AND INTERFERENCES
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